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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/068,014	02/05/2002	Keith A. Joyner	TI-29912	7239

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TEXAS INSTRUMENTS INCORPORATED
P O BOX 655474, M/S 3999
DALLAS, TX 75265

EXAMINER
BREWSTER, WILLIAM M

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 07/23/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application N .	Applicant(s)	
	10/068,014	JOYNER ET AL.	
	Examiner	Art Unit	
	William M. Brewster	2823	

-- The MAILING DATE of this communication appears on the c ver sheet with the correspondence address --

Period f r Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 May 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disp sition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) *15-25* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 8-10, 12-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chau et al., U.S. Patent No. 6,165,826 in view of Tsai et al., U.S. Patent No. 5,757,045.

Chau teaches a method for manufacturing a transistor, comprising: in fig. 3A, providing a transistor assembly including a silicon based semiconductor layer 300 with a first surface, above label 301, a dielectric layer 303 disposed on at least part of the first surface, and a gate electrode 306 disposed on the dielectric layer,

limitations from claims 9 & 10: in fig. 3B, further comprising applying a dopant to a portion of the first surface to form a source region 312, wherein applying a dopant comprises diffusing arsenic into the portion of the first surface, col. 6, line 58 - col. 7, line 8;

in fig. 3D, the assembly further including an insulation layer 314 adjacent at least part of the gate electrode and, in fig. 3F, a nitride spacer layer 326 adjacent at least part of the

insulation layer; in fig. 3H, depositing, on a portion of the first surface, a material that will react with the semiconductor layer to form silicide and removing the unreacted material, col. 11, line 66 - col. 12, line 26;

limitations from claim 14: in fig. 3H, wherein depositing a material that will react with the semiconductor layer to form silicide comprises depositing the material on an exposed surface of the gate electrode to form a silicided portion of the gate electrode 342, see above cite;

in fig. 3G, etching the nitride spacer layer;

limitations from claim 12: in fig. 3G, removing a portion of the nitride spacer layer to expose part of a surface of the insulation layer 324 (inherently needed to etch 326 before etching 324); and removing the portion of the insulation layer below the exposed surface 301 of the insulation layer to expose part of the first surface of the semiconductor layer, col. 11, line 66 - col. 12, line 26.

Chau states using "conventional and well known processes" for forming interconnects in col. 12, lines 27-33, but does not elaborate said methods. Tsai, however, does elaborate on forming interconnects. Tsai teaches a method for manufacturing a transistor, comprising: in fig. 3, providing a transistor assembly including a silicon based semiconductor layer 1 with a first surface, a dielectric layer 11 disposed on at least part of the first surface, and a gate electrode 12 disposed on the dielectric layer, in fig. 7, the assembly further including an insulation layer 13 adjacent at least part of the gate electrode and a nitride spacer layer 14 adjacent at least part of the

insulation layer, col. 4, line 52 - col. 5, line 2; limitations from claims 9 & 10: in fig. 5, further comprising applying a dopant to a portion of the first surface to form a source region, wherein applying a dopant comprises diffusing arsenic into the portion 16 of the first surface, col. 5, lines 3 - 24; in fig. 7, depositing, on a portion of the first surface, a material that will react with the semiconductor layer to form silicide, col. 5, lines 23-64; limitations from claim 14: in fig. 7, wherein depositing a material that will react with the semiconductor layer to form silicide comprises depositing the material on an exposed surface of the gate electrode to form a silicided portion of the gate electrode 19, col. 5, lines 23-64; in fig. 8, removing the unreacted material; etching the nitride spacer layer; limitations from claim 8: wherein an edge of the contact is formed between approximately forty to one-hundred and fifty nanometers from an edge of the gate electrode, the spacer thickness is 1000 - 3000 Å, and most of it is removed, col. 4, line 52 - col. 5, line 2; in fig. 13, depositing a pre-metal spacer layer 28 adjacent at least part of the nitride spacer layer and at least part of the silicided portion of the first surface; etch removing a portion 29 of the pre-metal spacer layer above the silicided portion 19 of the first surface to expose at least part of the silicided portion of the first surface; and forming a contact 30 with the exposed part of the silicided portion of the first surface where the pre-metal spacer layer was removed, col. 7, lines 1 - 21; limitations from claim 13: further comprising: depositing a second pre-metal spacer (14 the symmetric side of the gate opposite to the spacer layer also labeled 14) layer adjacent the first pre-metal spacer layer; and etching a portion of the second pre-metal spacer layer above at least part of the silicided portion of the first surface to expose a

part of a surface of the first pre-metal spacer layer. Tsai gives motivation in col. 1, line 56 - col. 2, line 8. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to recognize that combining Tsai's process with Chau's invention would have been beneficial because it allows for connections from an ultra shallow ion implantation region to produce a quarter micron CMOS device.

Claims 2-7, 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsai as applied to claims 1, 8-10 above, and further in view of Wolf, V. I, pp. 144-47, 534.

Neither Chau nor Tsai specify using cobalt for silicide, or phosphoric acid for etching the nitride spacer material, but Wolf teaches both. Wolf teaches on page 534, etching nitride wherein the etchant comprises phosphoric acid, wherein the temperature of the etchant comprises approximately one-hundred and sixty degrees Celsius, 180° C, at an etch rats of about 100 Å/min, or between two to eight minutes for tens of nanometers. The etchant would be rinsed and dried from the device in order to prevent failures of the device later on in the field. On pp. 144-47, Wolf teaches forming silicide contacts from cobalt. Wolf gives motivation on p. 147, 3rd ¶. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to recognize that combining Wolf's process with Chau and Tsai's invention would have been beneficial because $CoSi_2$ exhibits one of the lowest resistivities of the silicides.

Chau nor Tsai does not specify the limitations from claim 2: wherein etching the nitride spacer layer comprises reducing the width of the nitride spacer layer approximately thirty nanometers. However, such dimensions may be optimized.

"Normally, it is to be expected that a change in temperature, or in concentration, or in both, would be an unpatentable modification. Under some circumstances, however, changes such as these may impart patentablility to a process if the particular ranges claimed produce a new and unexpected result which is different in kind and not merely degree from the results of the prior art . . . such ranges are termed 'critical ranges' and the applicant has the burden of proving such criticality . . . More particularly, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation."

> In re Aller 105 USPQ 233, 255 (CCPA 1955). See also In re Waite 77 USPQ 586 (CCPA 1948); In re Scherl 70 USPQ 204 (CCPA 1946); In re Irmscher 66 USPQ 314 (CCPA 1945); In re Norman 66 USPQ 308 (CCPA 1945); In re Swenson 56 USPQ 372 (CCPA 1942); In re Sola 25 USPQ 433 (CCPA 1935); In re Dreyfus 24 USPQ 52 (CCPA 1934).

Note that the specification contains no disclosure of either the critical nature of the claimed dimensions of any unexpected results arising there from. Where patentability is aid to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Response to Arguments

Applicant's arguments with respect to all claims have been considered but are moot in view of the new ground(s) of rejection. Chau teaches the etching of the nitride spacer, and Tsai teaches the forming of a pre-metal spacer layer.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to William M. Brewster whose telephone number is 703-305-5906. The examiner can normally be reached on Full Time.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 703-306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are 703-305-3432 for regular communications and 703-305-3432 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

WB
July 2, 2003

Olik Chaudhuri
Supervisory Patent Examiner
Technology Center 2800